23

tab networks.

<u>CLAIMS</u>

What is claimed is:

1	1. A layout of a programmable logic device comprising a plurality
2	of configurable function generators (CFG) and storage elements, said layout
3	comprising:
4	a plurality of blocks, each block comprising a plurality of CFGs and
5	storage elements, said blocks paired to a first adjacent block that is adjacent
6	in a first direction and a second adjacent block that is adjacent in a second
7	direction;
8	a first block connector tab network coupled to each block of the
9	plurality of blocks that programmably couples in the first direction the CFGs
10	of the block to routing lines of the device and a second block connector tab
11	network coupled to each block of the plurality of blocks that programmably
12	couples in the second direction the CFGs of the block to routing lines of the
13	device, the first and second block connector tab networks of paired blocks
14	oriented to mirror images of each other, each of said first and second said
15	block connector tab networks comprising a memory and passgate array for
16	forming a plurality of programmable connections and driver logic for
17	driving signals, the memory and passgate arrays of paired blocks combined
18	into a single array; and
19	a turn network for programmably coupling routing lines, said turn
20	network comprising a memory and passgate array, said memory and
21	passgate array of the turn network contiguous to the memory and passgate
22	arrays of the first block connector tab networks and second block connector

1	2. The layout as set forth in claim 38, wherein a block comprises a
2	plurality of logic clusters, each logic cluster comprising a set of the plurality
3	of CFGs and storage elements programmably interconnected via a cluster
4	routing matrix composed of intracluster routing lines and programmable
5	switches, a layout within each block comprising:
6	a memory and passgate array comprising;
7	a first portion comprising memory and passgates corresponding
8	to switches of the cluster routing matrix of each logic cluster of the
9	block;
10	a second portion comprising memory and passgates
11	corresponding to switches of extensions which programmably couples
12	cluster routing matrices of adjacent clusters within the block;
13	a third portion comprising memory and passgates
14	corresponding to switches which programmably couple CFGs to block
15	connectors, said block connectors programmably coupled to the block
16	connector tab networks; and
17	a plurality of logic arrays, each logic array corresponding to the CFGs
18	of a cluster, said logic arrays located external to the area spanned by the
19	memory and passgate array.